Introduction to VLSI Design

- Instructor: Steven P. Levitan
  steve@ece.pitt.edu
- TA: Gayatri Mehta, Jose Martinez
- Book: Digital Integrated Circuits: A Design Perspective; Jan Rabaey
- Lab Notes: Handed out
Course Outline (approximate)

- Introduction and Motivation
- The VLSI Design Process
- Details of the MOS Transistor
- Device Fabrication
- Design Rules
- CMOS circuits
- VLSI Structures
- System Timing
- Real Circuits and Performance
Reference Books

- *Digital Integrated Circuits: A Design Perspective* Rabaey et. al
- *CMOS VLSI Design A Circuits and Systems Perspective* (3rd Edition) Neil Weste and David Harris Addison Wesley
- *Introduction to VLSI Circuits and Systems* Uyemura
- More – on reserve in the Library
  - Chen, Smith, Sedra & Smith, etc.
Software

– Cadence “icfb”
  ● Schematic and Layout editors
  ● Unix Based
  ● Some Auto-Layout generation
  ● Batch Design Rule Checking
  ● Circuit Extraction - LVS
  ● Many Supported Technology files

– HSPICE
  ● Based on well known SPICE (HSPICE is better)
  ● Good support/documentation
  ● Interface with both schematic and Layout

– Verilog / (later)
  ● High level design and evaluation
  ● Fast functional validation
  ● Synthesis from Verilog to circuit to layout

– Others
  ● Micro Magic Max and Sue and Data Path Compiler
Digital Integrated Circuits
A Design Perspective

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

Introduction
July 30, 2002
What is this book all about?

- Introduction to digital integrated circuits.

- What will you learn?
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: cost, speed, power dissipation, and reliability.
Digital Integrated Circuits

- Introduction: Issues in digital design
- The CMOS inverter
- Combinational logic structures
- Sequential logic gates
- Design methodologies
- Interconnect: R, L and C
- Timing
- Arithmetic building blocks
- Memories and array structures
Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in the future?
The First Computer

The Babbage Difference Engine (1832)
25,000 parts
cost: £17,470
ENIAC - The first electronic computer (1946)

The first electronic computer (1946)

Electronic Numerical Integrator and Computer

© Digital Integrated Circuits 2nd Introduction
The Transistor Revolution

First transistor
Bell Labs, 1948
FIG 1.2 (a) First transistor (Courtesy of Texas Instruments.) and (b) first integrated circuit. (Property of AT&T Archives. Reprinted with permission of AT&T.)
The First Integrated Circuits

Bipolar logic
1960’s
6 Transistors
5 Resistors
True and complement outputs

ECL 3-input Gate
Motorola 1966
FIG 1.3 (a) Intel 1101 SRAM (© IEEE 1967 [Vadasz69]) and (b) 4004 microprocessor (Reprinted with permission of Intel Corporation.)
Intel 4004 Micro-Processor

1971
1000 transistors
1 MHz operation
Intel Pentium (IV) microprocessor

2001
40M Transistors
100MHz (?)
Moore’s Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months.
Moore’s Law


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Introduction
FIG 1.4 Transistors in Intel microprocessors [Intel03]
Transistor Counts

1 Billion Transistors

Source: Intel

Projected

© Digital Integrated Circuits 2nd

Courtesy, Intel

Introduction
Moore’s law in Microprocessors

Transistors on Lead Microprocessors double every 2 years

2X growth in 1.96 years!

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Introduction

Courtesy, Intel
Die Size Growth

Die size grows by 14% to satisfy Moore’s Law

~7% growth per year
~2X growth in 10 years

© Digital Integrated Circuits 2nd
Courtesy, Intel
Introduction
Frequency

Doubles every 2 years

Lead Microprocessors frequency doubles every 2 years

© Digital Integrated Circuits 2nd

Courtesy, Intel

Introduction
Evolution in Complexity

The chart illustrates the evolution in complexity over time, with the x-axis representing the year from 1970 to 2010 and the y-axis showing the number of bits per chip. Key points include:

- **1970**: 64 Kbits, 1.6-2.4μm
- **1980**: 256 Kbits, 1.0-1.2μm
- **1990**: 64 Mbits, 0.35-0.4μm
- **2000**: 1 Gbit, 0.15-0.2μm
- **2010**: 4 Gbits, 0.08μm

Notable milestones include:

- Human DNA
- Human memory
- Book
- Encyclopedia
- 2 hrs CD Audio
- 30 sec HDTV

This evolution reflects significant advancements in digital integrated circuits.
Power Dissipation

Lead Microprocessors power continues to increase

© Digital Integrated Circuits 2nd

Courtesy, Intel

Introduction
Power will be a major problem

Power delivery and dissipation will be prohibitive
Power density too high to keep junctions at low temp

Power density

Power Density (W/cm²)

10000
1000
100
10
1

Year


Hot Plate

Rocket Nozzle

Nuclear Reactor

Pentium® proc

Power density too high to keep junctions at low temp

© Digital Integrated Circuits 2nd

Courtesy, Intel

Introduction
Not Only Microprocessors

Cell Phone

Digital Cellular Market (Phones Shipped)

<table>
<thead>
<tr>
<th>Year</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1996</td>
<td>48M</td>
</tr>
<tr>
<td>1997</td>
<td>86M</td>
</tr>
<tr>
<td>1998</td>
<td>162M</td>
</tr>
<tr>
<td>1999</td>
<td>260M</td>
</tr>
<tr>
<td>2000</td>
<td>435M</td>
</tr>
</tbody>
</table>

(data from Texas Instruments)
Challenges in Digital Design

“Giga = 1/Nano”

∞ DSM

“Microscopic Problems”
• Ultra-high speed design
• Interconnect
• Noise, Crosstalk
• Reliability, Manufacturability
• Power Dissipation
• Clock distribution.

Everything Looks a Little Different

∞ 1/DSM

“Macroscopic Issues”
• Time-to-Market
• Millions of Gates
• High-Level Abstractions
• Reuse & IP: Portability
• Predictability
• etc.

…and There’s a Lot of Them!
CMOS: Complementary MOS

- Means we are using both N-channel and P-channel type enhancement mode Field Effect Transistors (FETs).
- Field Effect - NO current from the controlling electrode into the output
  - FET is a voltage controlled current device
    vs. BJT (which is a current controlled current device)
- N/P Channel - doping of the substrate for increased carriers (electrons or holes)
**Silicon Doping**

*Group V atoms: Phosphorus or Arsenic, one more electron → n-type*

*Group III atoms: Boron, one less electron → p-type*

*Doping concentrations: 10e-5 (strong) to 10e-8 (weak)*

---

(a) ![Diagram of Silicon lattice and dopant atoms](image)

(b) ![Diagram of Silicon lattice and dopant atoms](image)

(c) ![Diagram of Silicon lattice and dopant atoms](image)

**FIG 1.6** Silicon lattice and dopant atoms
N-Channel Enhancement mode MOS FET

- Four Terminal Device - substrate bias

Diagram showing the N-channel enhancement mode MOSFET with labels for gate, source, drain, substrate, and gate oxide.
FIG 1.10 Inverter schematic (a) and symbol (b) $Y = \overline{A}$
VLSI: Very Large Scale Integration

- Integration: Integrated Circuits
  - multiple devices on one substrate

- How large is Very Large?
  - SSI (small scale integration)
    - 7400 series, 10-100 transistors
  - MSI (medium scale)
    - 74000 series 100-1000
  - LSI 1,000-10,000 transistors
  - VLSI > 10,000 transistors (original definition)
  - ULSI/SLSI (some disagreement, VLSI > 10M)
VLSI Design

– But the real issue is that VLSI is about designing systems on chips.
– The designs are complex, and we need to use structured design techniques and sophisticated design tools to manage the complexity of the design.
– We also accept the fact that any technology we learn the details of will be out of date soon.
– We are trying to develop and use techniques that will transcend the technology, but still respect it.
The Process of VLSI Design:

Consists of many different representations/Abstractions of the system (chip) that is being designed.

– System Level Design
– Architecture / Algorithm Level Design
– Digital System Level Design
– Logical Level Design
– Electrical Level Design
– Layout Level Design
– Semiconductor Level Design (possibly more)

Each abstraction/view is itself a Design Hierarchy of refinements which decompose the design.
Help from Computer Aided Design tools

- **Tools**
  - Editors
  - Simulators
  - Libraries
  - Module Synthesizers
  - Placers/Routers
  - Chip Assemblers
  - Silicon Compilers

- **Experts**
  - Logic design
  - Electronic/circuit design
  - Device physics
  - Artwork
  - Applications - system design
  - Architectures
New Design Methodologies

- Methodologies which are based on:
  - System Level Abstractions v.s. Device Characteristic Abstractions
    - Logic structures and circuitry change slowly over time
      - trade-offs do change, but the choices do not
  - Scalable Designs
    - Layout techniques also change slowly.
      - But the minimum feature size steadily decreases with time (also Voltage, Die Size, etc.)
Technologies

- Bipolar (BJT) dual Junction, current controlled devices
  - TTL, Schottky
  - ECL
  - $I^2$L

- Voltage controlled devices
  - Metal Oxide Silicon Field Effect Transistors (MOS FET)
    - NMOS, PMOS (enhancement, depletion)
    - CMOS <= our course

- Single Junction voltage controlled devices
  - GaAs (typically JFET’s)
  - OEIC’s - MQW’s, Integrated Lasers,
Design Approaches

- Custom
  - full control of design
  - best results, slowest design time.

- Semi-custom (std cell)
  - use Cell libraries from vendor
  - cad tools, faster design time

- Gate Array
  - fastest design time
  - worst speed/power/density
  - best low volume (worst high volume)

- EPLA/EPLD - FPGA - electrically programmable (in the field) -
Productivity Trends

Complexity outpaces design productivity

Source: Sematech

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Courtesy, ITRS Roadmap

Introduction
Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly (effective area grows by 2x)
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction
Design Abstraction Levels
Figure 1.2 (p.4) General overview of the design hierarchy.

- Top design level: System specifications
  - Initial concept
  - System design and verification
- Abstract high-level model: VHDL, Verilog HDL
- Logic synthesis
- Circuit design
- CMOS design and verification
- Physical design
- Silicon logic design and verification
- Manufacturing
- Mass production, testing, and packaging
- Finished VLSI chip
- Marketing

Introduction to Circuits, Fourth Edition by Peter Uyemura, Copyright © 2004 John Wiley & Sons. All rights reserved.
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Area
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function
Cost of Integrated Circuits

- **NRE** (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor

- **Recurrent costs**
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area
**NRE Cost is Increasing**

- "The club of people who can afford an extreme sub-micron ASIC or COTS design is getting pretty exclusive."
  - Ron Wilson, EE Times (May 2000)

![Graph showing increasing NRE costs over time](chart)

- 70nm ASICs will have $4M NRE.
**Die Cost**

Going up to 12” (30cm)

From http://www.amd.com

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Introduction
Cost per Transistor

Fabrication capital cost per transistor (Moore’s law)
Yield

\[ Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\% \]

Die cost = \[ \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}} \]

Dies per wafer = \[ \frac{\pi \times \left( \text{wafer diameter}/2 \right)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}} \]
Defects

\[
die\ yield = \left( 1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}
\]

\(\alpha\) is approximately 3

\[
die\ cost = f(\text{die area})^4
\]
# Some Examples (1994)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Def./cm²</th>
<th>Area mm²</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486 DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>Power PC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super Sparc</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
ITRS Technology “nodes”

International Technology Roadmap for Semiconductors

http://www.itrs.net/

Sponsored by the five leading chip manufacturing regions in the world: Europe, Japan, Korea, Taiwan, and the United States. The objective of the ITRS is to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices, thereby continuing the health and success of this industry. --- “Moore’s Law Police”

<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Calculated Trend Numbers (nm)</td>
<td>360</td>
<td>255</td>
<td>180</td>
<td>127.3</td>
<td>101</td>
<td>90</td>
<td>71.4</td>
<td>63.6</td>
<td>50.5</td>
<td>45</td>
<td>35.7</td>
<td>31.8</td>
<td>25.3</td>
<td>22.5</td>
<td>17.9</td>
<td>15.9</td>
</tr>
<tr>
<td>ITRS Rounded Numbers (nm)</td>
<td>350</td>
<td>250</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>90</td>
<td>70</td>
<td>65</td>
<td>50</td>
<td>45</td>
<td>36</td>
<td>32</td>
<td>25</td>
<td>22</td>
<td>18</td>
<td>16</td>
</tr>
</tbody>
</table>
MOS Transistor Scaling
(1974 to present)

\[ S = 0.7 \]

[0.5x per 2 Technology Cycles]

Figure 6  MOS Transistor Scaling—1974 to present

THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: 2005
Scaling Calculator +

Cycle Time:

250 → 180 → 130 → 90 → 65 → 45 → 32 → 22 → 16

N-1  N  N+1

0.7x  0.7x  0.5x

1994 NTRS - .7x/3yrs
Actual - .7x/2yrs
Linear Time

Cycle Time
(T yrs):
*CARR(T) =
[(0.5)^((1/2T yrs))] - 1
CARR(3 yrs) = -10.9%
CARR(2 yrs) = -15.9%

* CARR(T) = Compound Annual Reduction Rate
(@ cycle time period, T)

(DRAM M1 Example)

Figure 7  Scaling Calculator

THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS:  2005
<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM ⅓ Pitch (nm) (contacted)</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) ⅓ Pitch (nm) (f)</td>
<td>90</td>
<td>78</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>23</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td>Affordable Cost per Function ++</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAM cost/bit at (packaged microcents) at samples/introduction</td>
<td>5.3</td>
<td>3.7</td>
<td>2.6</td>
<td>1.9</td>
<td>1.3</td>
<td>0.93</td>
<td>0.66</td>
<td>0.46</td>
<td>0.33</td>
</tr>
<tr>
<td>DRAM cost/bit at (packaged microcents) at production §</td>
<td>1.9</td>
<td>1.4</td>
<td>0.96</td>
<td>0.68</td>
<td>0.48</td>
<td>0.34</td>
<td>0.24</td>
<td>0.17</td>
<td>0.12</td>
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<tr>
<td>Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§</td>
<td>44.0</td>
<td>31.1</td>
<td>22.0</td>
<td>15.6</td>
<td>11.0</td>
<td>7.8</td>
<td>5.5</td>
<td>3.9</td>
<td>2.8</td>
</tr>
<tr>
<td>Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§</td>
<td>26.6</td>
<td>18.8</td>
<td>13.3</td>
<td>9.4</td>
<td>6.7</td>
<td>4.7</td>
<td>3.3</td>
<td>2.4</td>
<td>1.7</td>
</tr>
<tr>
<td>High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§</td>
<td>24.4</td>
<td>17.2</td>
<td>12.2</td>
<td>8.6</td>
<td>6.1</td>
<td>4.3</td>
<td>3.0</td>
<td>2.2</td>
<td>1.5</td>
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### Table 6a  Power Supply and Power Dissipation—Near-term Years

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2005</th>
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<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM ½ Pitch (nm) (contacted)</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
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<tr>
<td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)</td>
<td>90</td>
<td>78</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
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<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>23</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td>Power Supply Voltage (V)</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Vdd (high-performance)</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
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<tr>
<td>Vdd (Low Operating Power, high Vdd transistors)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.6</td>
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<td>Allowable Maximum Power [1]</td>
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<tr>
<td>High-performance with heatsink (W)</td>
<td>167</td>
<td>180</td>
<td>189</td>
<td>198</td>
<td>198</td>
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<tr>
<td>Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation</td>
<td>310</td>
<td>310</td>
<td>310</td>
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<td>310</td>
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</tr>
<tr>
<td>Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation</td>
<td>0.54</td>
<td>0.58</td>
<td>0.61</td>
<td>0.64</td>
<td>0.64</td>
<td>0.64</td>
<td>0.64</td>
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<td>Cost-performance (W)</td>
<td>91</td>
<td>98</td>
<td>104</td>
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<td>116</td>
<td>119</td>
<td>119</td>
<td>125</td>
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<tr>
<td>Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation</td>
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<td>140</td>
<td>140</td>
<td>140</td>
<td>140</td>
<td>140</td>
<td>140</td>
<td>140</td>
<td>140</td>
</tr>
<tr>
<td>Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation</td>
<td>0.65</td>
<td>0.70</td>
<td>0.74</td>
<td>0.79</td>
<td>0.83</td>
<td>0.85</td>
<td>0.85</td>
<td>0.89</td>
<td>0.98</td>
</tr>
<tr>
<td>Battery (W)—(low-cost/hand-held)</td>
<td>2.8</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
</tr>
</tbody>
</table>

[1] Power will be limited more by system level cooling and test constraints than packaging.
### Table 4c  Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM 1/2 Pitch (nm) (contacted)</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm) (f)</td>
<td>90</td>
<td>78</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>23</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td><strong>Chip Frequency (MHz)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip local clock [1]</td>
<td>5,204</td>
<td>6,783</td>
<td>9,285</td>
<td>10,972</td>
<td>12,369</td>
<td>15,079</td>
<td>17,658</td>
<td>20,065</td>
<td>22,980</td>
</tr>
<tr>
<td>Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[2]</td>
<td>3,125</td>
<td>3,906</td>
<td>4,883</td>
<td>6,103</td>
<td>7,629</td>
<td>9,536</td>
<td>11,920</td>
<td>14,900</td>
<td>18,625</td>
</tr>
<tr>
<td>Maximum number wiring levels—maximum [3]</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>17</td>
</tr>
<tr>
<td>Year of Production</td>
<td>2005</td>
<td>2006</td>
<td>2007</td>
<td>2008</td>
<td>2009</td>
<td>2010</td>
<td>2011</td>
<td>2012</td>
<td>2013</td>
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<td>------</td>
</tr>
<tr>
<td>DRAM ½ Pitch (nm) (contacted)</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)</td>
<td>90</td>
<td>78</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
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<td>23</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
</tr>
</tbody>
</table>

**Number of Chip I/Os (Number of Total Chip Pads)—Maximum**

<table>
<thead>
<tr>
<th>Total pads—MPU</th>
<th>3,072</th>
<th>3,072</th>
<th>3,072</th>
<th>3,072</th>
<th>3,072</th>
<th>3,072</th>
<th>3,072</th>
<th>3,072</th>
<th>3,072</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal I/O—MPU (1/3 of total pads)</td>
<td>1,024</td>
<td>1,024</td>
<td>1,024</td>
<td>1,024</td>
<td>1,024</td>
<td>1,024</td>
<td>1,024</td>
<td>1,024</td>
<td>1,024</td>
</tr>
<tr>
<td>Power and ground pads—MPU (2/3 of total pads)</td>
<td>2,048</td>
<td>2,048</td>
<td>2,048</td>
<td>2,048</td>
<td>2,048</td>
<td>2,048</td>
<td>2,048</td>
<td>2,048</td>
<td>2,048</td>
</tr>
<tr>
<td>Total pads—ASIC high-performance</td>
<td>4,000</td>
<td>4,200</td>
<td>4,400</td>
<td>4,400</td>
<td>4,600</td>
<td>4,800</td>
<td>4,800</td>
<td>5,000</td>
<td>5,400</td>
</tr>
<tr>
<td>Signal I/O pads—ASIC high-performance</td>
<td>2,000</td>
<td>2,100</td>
<td>2,200</td>
<td>2,200</td>
<td>2,300</td>
<td>2,400</td>
<td>2,400</td>
<td>2,500</td>
<td>2,700</td>
</tr>
<tr>
<td>Power and ground pads—ASIC high-performance (½ of total pads)</td>
<td>2,000</td>
<td>2,100</td>
<td>2,200</td>
<td>2,200</td>
<td>2,300</td>
<td>2,400</td>
<td>2,400</td>
<td>2,500</td>
<td>2,700</td>
</tr>
</tbody>
</table>

**Number of Total Package Pins—Maximum [1]**

<table>
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<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Microprocessor/controller, high-performance</td>
<td>900</td>
<td>990</td>
<td>1088</td>
<td>1198</td>
<td>1318</td>
<td>1450</td>
<td>1596</td>
<td>1754</td>
<td>1930</td>
</tr>
<tr>
<td>ASIC (high-performance)</td>
<td>3000</td>
<td>3180</td>
<td>3371</td>
<td>3573</td>
<td>3787</td>
<td>4015</td>
<td>4256</td>
<td>4511</td>
<td>4736</td>
</tr>
<tr>
<td></td>
<td>2005</td>
<td>2006</td>
<td>2007</td>
<td>2008</td>
<td>2009</td>
<td>2010</td>
<td>2011</td>
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<td>16</td>
<td>14</td>
<td>13</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Logic (Low-volume Microprocessor) High-performance d</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Generation at Introduction</strong></td>
</tr>
<tr>
<td><strong>Functions per chip at introduction (million transistors)</strong></td>
</tr>
<tr>
<td><strong>Chip size at introduction (mm²)</strong></td>
</tr>
<tr>
<td><strong>Generation at production d</strong></td>
</tr>
<tr>
<td><strong>Functions per chip at production (million transistors)</strong></td>
</tr>
<tr>
<td><strong>Chip size at production (mm²) d</strong></td>
</tr>
<tr>
<td><strong>High-performance MPU Mtransistors/cm² at introduction and production (including on-chip SRAM) d</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>ASIC</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ASIC usable Mtransistors/cm² (auto layout)</strong></td>
</tr>
<tr>
<td><strong>ASIC max chip size at production (mm²) (maximum lithographic field size)</strong></td>
</tr>
<tr>
<td><strong>ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)</strong></td>
</tr>
</tbody>
</table>
2005 ITRS Product Function Size Trends -
Cell Size, Logic Gate(4t) Size

- DRAM Cell Size (u2)
- Flash Cell Size (u2)
  SLC (NEW)
- Flash Eqv.bit Size(u2)
  MLC (NEW)
- MPU SRAM Cell Size
  (6t)(u2)
- MPU Gate Size (4t)(u2)

Note for Flash:
SLC = Single-Level-Cell Size
MLC = Multi-Level-Cell
(Electrical Equivalent) Cell Size

2005 - 2020 ITRS Range

Figure 9  2005 ITRS Product Function Size Trends:
The International Technology Roadmap for Semiconductors: 2005
Figure 10  2005 ITRS Product Technology Trends:  
Product Functions/Chip and Industry Average “Moore’s Law” Trends
Silicon in 2010

Voltage: 0.7 - 1.0 V
Technology: 0.045 μm
Metal layers: 12-16
Clock: 10-15GHz
Metal Pitch: 45nm
Active length: 30nm/18nm (38/23nm low power)
DRAM: 32Gbit on 24x24mm die
Logic Transistors: 6G on 30x30mm die
Pins: 1,000 – 4,000 (66% Power Pins)
Power: 100-200W
Wafer Size: 12” diameter
“more than Moore”
Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this book
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation
Reliability—
Noise in Digital Integrated Circuits

Inductive coupling

Capacitive coupling

Power and ground noise

i(t)

v(t)

V_{DD}
DC Operation
Voltage Transfer Characteristic

$V_OH = f(VOL)$
$VOL = f(VOH)$
$VM = f(VM)$

Switching Threshold
Nominal Voltage Levels
Mapping between analog and digital signals

“1”

- \( V_{OH} \)
- \( V_{IH} \)

Undefined Region

“0”

- \( V_{IL} \)
- \( V_{OL} \)

Slope = -1

V_{out} vs V_{in}

\( V_{OH} \)

Slope = -1

\( V_{IL} \) \( V_{IH} \)

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Introduction
Definition of Noise Margins

- **Noise margin high**
  - $V_{IH}$
  - $V_{IL}$
  - $\text{NM}_H$
  - Undefined Region

- **Noise margin low**
  - $V_{OH}$
  - $V_{OL}$
  - $\text{NM}_L$

- Gate Output → Gate Input
Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources
Key Reliability Properties

- Absolute noise margin values are deceptive
  - A floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)

- Noise immunity is the more important metric – the capability to suppress noise sources

- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;
Regenerative Property

Regenerative vs. Non-Regenerative

- **Regenerative**
  - Input: $v_0$
  - Output: $v_3$
  - Feature: $f(v)$

- **Non-Regenerative**
  - Input: $v_0$
  - Output: $v_3$
  - Feature: $f(v)$
Regenerative Property

A chain of inverters

Simulated response

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Fan-in and Fan-out

Fan-out $N$

Fan-in $M$
The Ideal Gate

- $R_i = \infty$
- $R_o = 0$
- Fanout = $\infty$
- $NM_H = NM_L = V_{DD}/2$

$$g = \infty$$
An Old-time Inverter

The graph shows a characteristic of an inverter, where the output voltage ($V_{out}$) is plotted against the input voltage ($V_{in}$). The graph includes two regions marked as $NM_L$ and $NM_H$, indicating the leakage current and high current regions, respectively. The point $V_M$ is a threshold voltage where the transition between the two states occurs.
Delay Definitions

Delay Definitions:

- $t_f$: rise time
- $t_r$: fall time
- $t_{pHL}$: propagation delay from high to low
- $t_{pLH}$: propagation delay from low to high

Graphs showing $V_{in}$ and $V_{out}$ over time with 10%, 50%, and 90% marks.
Ring Oscillator

\[ T = 2 \times t_p \times N \]
A First-Order RC Network

\[ v_{out}(t) = (1 - e^{-t/\tau}) V \]

\[ t_p = \ln(2) \tau = 0.69 \text{ RC} \]

Important model – matches delay of inverter
Power Dissipation

Instantaneous power:
\[ p(t) = v(t)i(t) = V_{\text{supply}}i(t) \]

Peak power:
\[ P_{\text{peak}} = V_{\text{supply}}i_{\text{peak}} \]

Average power:
\[ P_{\text{ave}} = \frac{1}{T} \int_t^{t+T} p(t)dt = \frac{V_{\text{supply}}}{T} \int_t^{t+T} i_{\text{supply}}(t)dt \]
**Energy and Energy-Delay**

Power-Delay Product (PDP) =

\[ E = \text{Energy per operation} = P_{av} \times t_p \]

Energy-Delay Product (EDP) =

\[ \text{quality metric of gate} = E \times t_p \]
A First-Order RC Network

\[ E_{0 \to 1} = \int_0^T P(t) \, dt = V_{dd} \int_0^T i_{\text{supply}}(t) \, dt = V_{dd} \int_0^T C_L \, dV_{out} = C_L \cdot V_{dd}^2 \]

\[ E_{\text{cap}} = \int_0^T P_{\text{cap}}(t) \, dt = \int_0^T V_{\text{out}} \cdot i_{\text{cap}}(t) \, dt = \int_0^T C_L \cdot V_{\text{out}} \, dV_{out} = \frac{1}{2} C_L \cdot V_{dd}^2 \]