Lab Assignment #9

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Department of Electrical and Computer Engineering
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Assignment (due Friday, November 10, 2006)

1 Introduction

The purpose of this lab assignment is to learn how to build **hierarchical designs** in **Data Path Compiler (DPC)** from Micro Magic tools. DPC runs on top of SUE and it converts SUE schematics into high performance data paths using icon positions, annotations, and hierarchy. It creates the following three files every time you run DPC:

(i) A verilog gate-level netlist
(ii) A DEF placement file
(iii) An estimated wire parasitic file

More information about the tool can be obtained from its tutorial and manual.

2 Setting up

- Make a **sub-directory** under **mmi_private** in your **home directory** and copy everything from **$CLASS/mmi_local/tech/** to **your sub-directory**.

```
> cd ~/mmi_private

> mkdir technology

> cd technology

> cp –R $CLASS/mmi_local/tech/* .
```

- *Note: You are using recursive copy command here (cp –R <source> <destination>).*

- Now you have a local copy of the standard cells and *a lot more stuff*.

- Now go back to your **mmi_private** directory and make a new sub-directory for the new lab and let's call it **"lab9"**. Also make different sub-directories for **sue** and **max** under **lab9**.

```
> cd ~/mmi_private/lab9/sue
```

```
> cp $CLASS/mmi_local/tech/mmi18/library/dpc/dpc.suerc .
```

- Now edit **dpc.suerc** by making the following changes to it:

  - **Comment** out the following lines with a **"#"** sign:
    ```
    set DPC_TIMING(pearl,command) pearl
    set DEFAULT_SPICE_HEADER $tech/spice/default_spice_header.h
    lappend DPC(PATH) $tech/library/dpc/$techtype.dpc
    ```

  - **Uncomment** the following line:
    ```
    set DPC_TIMING(simulator) "primetime"
    ```

  - **Add** the following line:
    ```
    lappend DPC(PATH) ./mmi18.dpc $tech/library/dpc/$techtype.dpc
    ```

- Now create a "**sue.rc"** file under **your sue directory** and add the following lines to it.
  ```
  set tech ~/mmi_private/technology/mmi18
  source ./dpc.suerc
  set GRID_SPACING "10 22"
  ```

- Now change directory to **"max"** under **lab9**.
  ```
  > cd ~/mmi_private/lab9/max
  ```

- Create a **".maxrc"** file under **your max directory** and add the following lines to it.
  ```
  mc_init
  cell_path_add ~/mmi_private/technology/mmi18/stdcell/max
  ```

3 Assignment

- You need to design a master-slave D flip-flop in sue using DPC by following the steps mentioned below and do the sub-tasks described as follows.

  - Create a schematic of a D-latch in sue and make its icon (Let's name it as "**Dlatch"**). Add the following line to the icon view in order to add the verilog property to it.

    ```
    type fixed –name verilog –text {Dlatch [unique_name "" $name
    Dlatch](.D($D),.clk($clk),.Q($Q),.Qbar($Qbar))\;}
    ```

  - **NOTE: Type the above command as one line. No carriage return.**

  - **NOTE: D and clk are the inputs and Q and Qbar are the outputs of the Dlatch. You've to use the names of the inputs and the outputs that you are using in your design. You've to use your design's name in the above command.**

  - Once you have a Dlatch, you need to do **DPC Netlist** and then you can view its placement view.

  - Now open another terminal and cd to **~/lab9/sue/.** Type the following command:

    ```
    > $CLASS/mmi_local/max_it.pl <design name>
    ```

- The above command will generate <**design name**>**.script.**
- Copy <**design name**>**.script** to **~/lab9/max/** directory.
- Open a max window and on the max terminal, type the following command:

  ```
  max> source <design name>.script
  ```

- Add a piece of **metal** and a **label** for inputs, outputs, vdd and gnd at the top-level of the design (*Top-level is* <***design name***> ***or Dlatch*** *for now*).
- Save your design with the same name you used in sue (e.g *Dlatch*).
- Measure the width and height of the Dlatch. Hint: In max window, first of all **turn all layers off** and **turn on prb** layer and then measure the width and height. It should be in multiples of **0.74** (Magic number). Suppose the size of your Dlatch is 7.4x7.4, then you need to divide both width and height by 0.74.
- Then create a new **mmi18.dpc** file in **~/mmi_private/lab9/sue/** and add the following line to the **mmi18.dpc** file

  ```
  <design name> width height
  ```

  e.g. Dlatch 10 10

- Do **Spice Convert** from the Local menu in max. Now you have max extracted netlist.
- Now go back to the **sue** directory. Design a **master-slave D flip-flop** using **D-latches** (***Use icons***). Now do **DPC Netlist** and look at its placement view.
- Now open another terminal and cd to **~/lab9/sue/.** Type the following command:

  ```
  > $CLASS/mmi_local/max_it.pl <design name>
  ```

- The above command will generate <**design name**>**.script.**
- Copy <**design name**>**.script** to **~/lab9/max/** directory.
- Open a max window and on the max terminal, type the following command:

  ```
  max> source <design name>.script
  ```

- Add a piece of **metal** and a **label** for inputs, outputs, vdd and gnd at the top-level of the design (*Top-level is* <***design name***> ***or Master-slave D flip-flop*** *for now*).
- Save your design with the same name you used in sue.
- Do **Spice Convert** from the Local menu in max. Now you have max extracted netlist.

- Create a **testbench** of a master-slave D flip-flop in **sue** and change the simulation mode to **"spice"**. Now simulate the master-slave D flip-flop using Local Schematics and Max-extracted netlist.

Turn in the printouts of the schematic view, placement view and layout of both D-latch and master-slave D flip-flop. Also turn-in the printouts of the waveforms.