# Lab Assignment #7



**University of Pittsburgh**
**Department of Electrical and Computer Engineering**
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## Assignment (due Friday, October 27, 2006)

1. Open the **sue tutorial** in browser and do the following sections from the tutorial:

   - **Part 3. Simulating Circuits with SPICE and IRSIM.** You had already done the **HSPICE sections** in one of the previous labs. **Do the IRSIM sections** this time. Use the **pulsegen testbench** for simulations. Do the following sections:
     - Running IRSIM
     - Interacting with IRSIM
     - Net names when netlisting
   - **Part 4. Higher Level Schematics and Verilog Simulation.** Do **all the sections except** the sections on **making and modifying an ICON** since you had already done these sections.

   You need to turn in the **printouts** of the **schematics** and the **simulation waveforms**.

2. You can also run **IRSIM** from the command prompt. Let's learn a few basic commands of **IRSIM** using the following script. We are considering a 2-input NAND-gate as an example here. An example script is as follows:

```
w a b out
vector in a b
ana a b in out
set in 00
s 20
set in 01
s 20
set in 10
s 20
set in 11
s 20
```

The **"w"** command tells IRSIM to watch the nodes in the following list ('a' and 'b' are the input nodes and 'out' is an output node). The **"vector"** command groups a list of inputs together so that these all can be set simultaneously. In the above script, input nodes 'a' and 'b' are grouped together in the vector 'in'. The **"ana"** (analyzer) command tells IRSIM to display the listed nodes and vector using its builtin graphical logic analyzer. The **"set in 00"** command is used to set the vector 'in' to '00' (a=0,b=0). The "s" command tells IRSIM to simulate for a certain period of time (in the above script it is 20 ns).

*Note: You can type the above given script in any text editor and save the above given script as **test.cmd**. You can save it using a different name but use **.cmd** as an extension.*

You already have a **2-input NAND-gate testbench** and the corresponding **.sim file** from the previous lab (Lab #6) that you can use here. Let's consider that you are in the **sue** folder and you have your NAND_tb.sim file there. In order to run IRSIM, type

```
irsim $MMI_TOOLS/sue/schematics/spice/hp-cmos26b.prm NAND_tb.sim –test.cmd
```

You need to turn in the **printout** of the **waveform**.

3. Now **simulate AND and OR gates** (which you had designed in Lab #6) using **IRSIM**. You need to simulate both **local schematics** and **max extracted netlists** in **sue** using the corresponding **testbenches** of these gates. **Use sue to get SIM netlists of these gates**. Once you have **.sim** files in the sue folder, type the above irsim command from Problem 2 to simulate these gates using IRSIM.

   ***Note: The only parts which are going to change in the command are the names of the .sim file and the .cmd file.***

   You had already simulated these gates using HSPICE in the previous lab. Now **compare** the waveforms you got using **HSPICE** and **IRSIM**.

   You need to turn in the **printouts** of the **waveforms** and a **brief explanation** of the waveforms.

4. Discuss briefly the differences between HSPICE and IRSIM simulations. You need to specify the differences that you have noticed while doing simulations using both simulators.