Lab Assignment #6

University of Pittsburgh
Department of Electrical and Computer Engineering
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Assignment (due Friday, October 20, 2006)

1. Open **max tutorial** in browser and do **MAX-LS section** from it. To do this, you need to design a schematic of a 2-input NAND gate in sue and name it as MyNAND. *Note: You can name it whatever you want to*. There are a few things that you need to do the way these are explained as follows instead of following the tutorial:
   - Create a directory for this assignment and two parallel sub-directories: max and sue
   - In the sue directory bring up a **sue** window by typing **sue** and design a 2-input NAND gate.
   - Go to the **Sim** menu and select **SIM netlist**. It's the top choice.
   - If the top choice is set to something else, like **spice netlist**, then select **change simulation mode** from the Sim menu and click on the **sim** box when the Change Simulation Mode dialog box comes up.
   - Now click on **SIM Netlist** from the **Sim** menu. **You will have MyNAND.sim in the sue folder.**
   - Now, in a new window, go to the max directory and bring up max window by typing **max.** Go to the **Tool** menu and click on **Layout Generator.**
   - When the file select popup appears, select **MyNAND.sim**. To find this you will have to go to the ../sue directory to find it in the the cell list.

   The Layout Generator will come up. This window has several options. **Now you can follow the tutorial for the rest of the work.**

2. In addition to the tutorial, design the following:
   NAND, NOR, AND, OR, XOR, AOI, OAI, Inverter

   The first five designs mentioned above have 2-inputs and 1-output. The AOI and OIA gats have three inputs and the inverter has a single-input and a single-output. Design all the gates as **symmetric gates** so that the **rise and fall times are equal.**

   To do Problem 2, create the **schematics** of the gates in **sue**. Now create the **testbenches** of the gates in **sue** and use a load of 30fF. Now **play in sue** to **optimize the transistor sizes** in order to get **symmetric gates**. Then generate the corresponding layouts **automatically using Layout Generator**

in max. **Verify the final layouts of the gates in max in the simulation.** For this, you need to simulate the max extracted netlists in sue.

You need to turn in the **printouts** of the **schematic view**, **layout view** and **simulation waveforms**.

3. Design two more NAND gates: (i) a NAND gate with 3-inputs, and (ii) a NAND gate with 4-inputs. Create the **schematics** of the gates in **sue**. Now create the **testbenches** of the gates in **sue** and use a load of 30fF. Now **play in sue** to **optimize the transistor sizes** in order to get **symmetric gates**. Then generate the corresponding layouts **automatically using Layout Generator in max**. **Verify the final layouts of the gates in max in the simulation.** For this, you need to simulate the max extracted netlists in sue.

   You need to turn in the **printouts** of the **schematic view**, **layout view** and **simulation waveforms**.