Lab Assignment #5

University of Pittsburgh
Department of Electrical and Computer Engineering
October 6, 2006 (Friday, Week 5)

1 Assignment (due Friday, October 13, 2006)

Note: For this assignment, use mmi20 technology library.

Type the following command in max window to change the technology library.

```
max –tech mmi20
```

1. This problem requires you to use a copy of your CMOS inverter from the previous lab.
   To do this problem,
   (a) first make $W_p=W_n$ for the inverter in **both sue and max** and simulate it using inverter's testbench (using local schematics and max extracted netlist). Use a pulse voltage source at the input terminal and a load of 30fF at the output terminal in the inverter testbench. Analyze the waveforms and **measure rise and fall times and propagation delay**.

   (b) now make $W_p=3W_n$ for the inverter in **both sue and max** and simulate it using inverter's testbench (using local schematics and max extracted netlist). Use a pulse voltage source at the input terminal and a load of 30fF at the output terminal in the inverter testbench. Analyze the waveforms and **measure rise and fall times and propagation delay.**

   Compare the waveforms you obtain for the Wp=Wn case with the Wp=3Wn case and comment on the changes in the rise and fall times and propagation delay, if any.

   You need to turn in the **printouts** of the **schematic view**, **layout view**, **simulation waveforms and a brief explanation of the waveforms**.

2. Design the circuit shown in Figure 1 in **both sue and max** and do cross-probing. Simulate the circuit using testbench in sue (using local schematics and max extracted netlist). Use a pulse voltage source at the input terminal in the testbench.
   Now measure
   (a) the delay from input A to output X
   (b) the delay from input A to output Y
   (c) the delay from input A to output Z

Also **compute the delays from input A to output X, input A to output Y and input A to output Z theoretically.**
You need to turn in **printouts** of the **schematic view**, **layout view** and **delay results**.

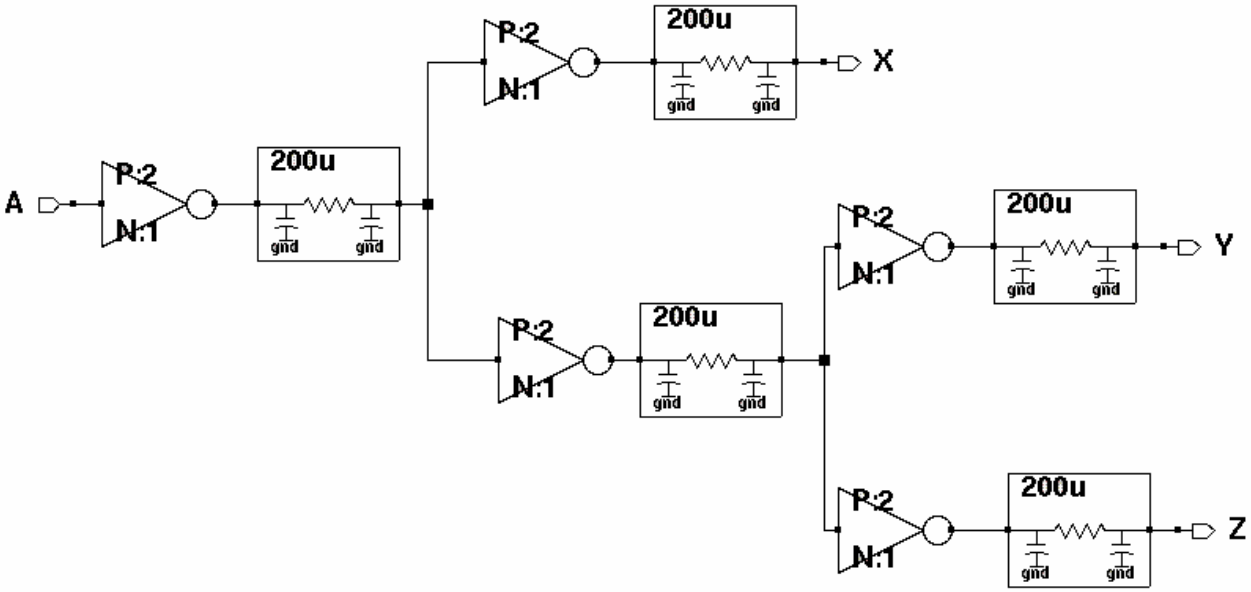

Figure 1.

Hint to do schematic of the above circuit in sue:

Use "**wireRC**" in sue for RC circuits shown above. Change the length of wireRC to 200 μm and use the default value of width (W=0.9 μm).

Hint to do layout of the above circuit in max:

Use poly instead of metal 1/metal 2 to draw wires of length 200 μm shown above as RC circuits. The reason for using poly is that it has higher resistance. Additional ideas about how to draw wires will be given during the lab session.

3. This problem is designed to explain the concept of **buffer insertion**. Design the circuits shown in Figures 2, 3 and 4 in **sue only** and simulate them using their respective testbenches. Use a pulse voltage source at the input terminal in all the testbenches. **Measure the delay from input A to output B in all three cases and comment on the difference in delay, if any.**

You need to turn in the **printouts** of the **schematic view, simulation waveforms and a brief explanation of the waveforms**.

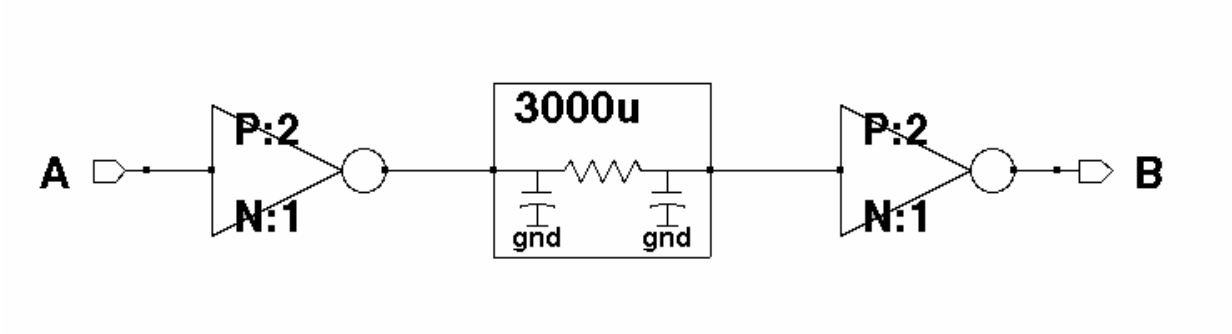

Figure 2.

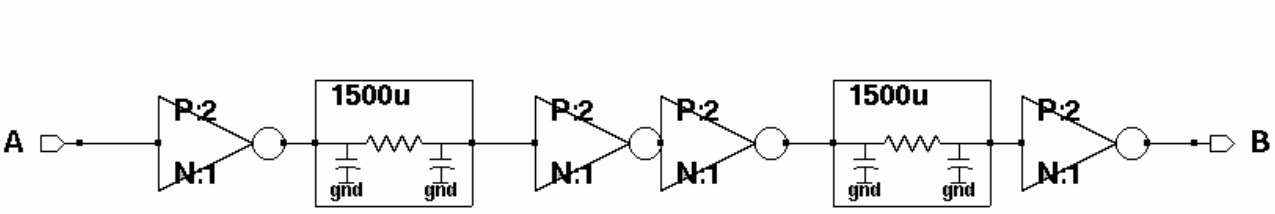

Figure 3.

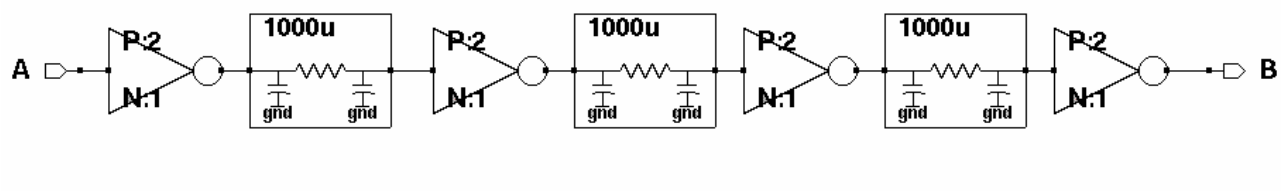

Figure 4.

Hint to do schematic of the above circuit in sue:

Use "**wireRC**" in sue for RC circuits shown above. Change the length of wireRC to 3000 μm, 1500 μm and 1000 μm for Figures 2, 3 and 4 respectively but use the default value of width (W=0.9 μm).