Lab Assignment #3

University of Pittsburgh
Department of Electrical and Computer Engineering
September 15, 2006 (Friday, Week 3)

1 Assignment (due Friday, September 22, 2006)

1. Plot an I_D vs. V_{DS} family of curves for a minimum size NMOS transistor (W=1u, L=0.5u). In your analysis, plot the output for five different V_{GS} voltages, eg. 1V, 1.5V, 2V, 2.5V and 3V. Note that you have to perform a DC sweep analysis on V_{DS} to plot the referred curves. *HINT:* In order to detect current through a specific net, connect a 0V voltage source (in series) on the net. The current through the 0V voltage source can be observed as the current through the net. **Repeat for PMOS making the correct changes in voltage values**

2. Illustrate short-circuit current during the switching of a CMOS inverter. Plot the output voltage, the input voltage, and the drain current, on the same graph. Assume a PULSE voltage input for this part. You can choose the pulse length, but do repeat the simulation for three different rise/fall times 10ps, 100ps, and 500ps. You must setup your circuits so that the input voltages cross the 50% point at the same time. Analyze the differences between the output currents when using different rise and fall times. Pay attention to the position in time when the current spikes, the area under the current curve and comment on the power dissipation.

3. This problem requires you to design a simple circuit that illustrates the fact that an NMOS transistor can not pass a high voltage well. To do this, you bias the transistor with $V_G=V_{DD}$, apply a PULSE voltage input (V_{in}) to the source, connect an output capacitor between drain and ground and connect the bulk to the ground i.e. V_B=0V. Assume an initial condition V_D=0 (the voltage across the capacitor). Plot the input voltage V_{in} and the output voltage V_D .
   NOTE: You will need to perform a transient analysis. Assume V_{DD}= 3V with an ideal step input at the source, and a 30fF load at the output terminal. **Repeat for PMOS making the correct changes for voltage values.**

Provide the following as your report:

Problem 1. Netlists, schematics and plots of NMOS **and PMOS** sweep operation

Problem 2. Netlist, schematic and plot for 10ps, 100ps and 500 ps. Compute the area under the current curves. Can you give us the power?

Problem 3. Netlists, schematics and plots of the transient operation for NMOS **and PMOS** circuits

For each problem, "netlist" means SPICE circuit, and you must provide a short explanation of each plot (2 to 3 sentences, at most per waveform)