Lab Assignment #6

University of Pittsburgh, Department of Electrical and Computer Engineering (Friday, Week 6)

Assignment (due Friday, October 15, 2008)
Add more cells to your standard cell library:

1. Schematic design a Flip-Flop as shown in Figure 7.19(b) in the 3rd edition of the book, which is figure 10.19(b) in the fourth edition.

Notes:

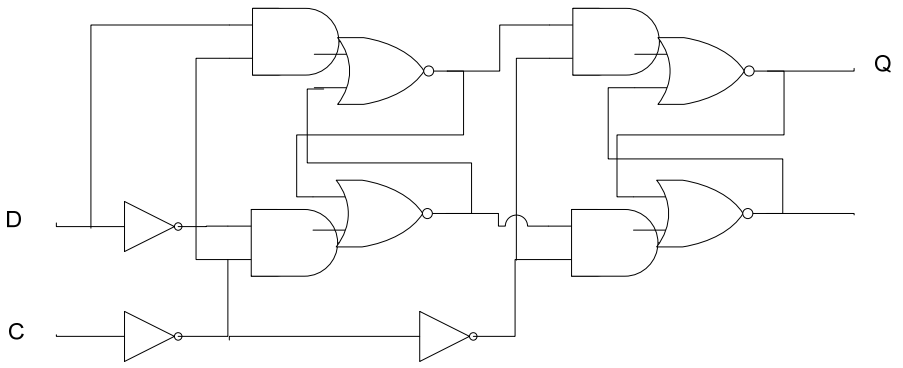
A. The pass gates do not have any connections to power or ground, none the less they must have well/substrate contacts in the well.
B. Carefully observe and label the two clock phases necessary
C. Add two inverters to the FF cell one to buffer clock and one to create phi_bar (~φ)

2. Schematic design a Flip-Flop as shown in Figure 7.21 (or 10.21) in the book.

Notes:

A. Carefully observe and label the four (4) clock phases necessary
B. Add four inverters to the FF cell to buffer the clock and create phi1_bar (~φ1), phi1_bar2 (~φ2)

3. Schematic design a Flip-Flop as shown below from four And-Or-Invert gates and 3 inverters:



4.

A. For Flip-flop 1 and 3 measure the setup time for both rising and falling inputs and include the T_{CQ} vs. T_{DC} plots to show the clock to output delay as a function of the clock setup time.
B. For Flip-flop 1 and 3, measure the hold time for both rising and falling inputs and include the T_{CQ} vs. T_{DC} plots to show the clock to output delay as a function of the clock hold time. HINT: you need another edge on D after the clock rising edge, which restores D to its starting value. T_{DC} here should be the delay from clock rising edge to this second edge of D. Make a large enough setup-time to not affect your hold time measurement!
C. For FF 1 and 3, plot T_{DQ} vs. T_{DC} for both rising and falling inputs to show the input to output delay. Find the optimum setup time with minimum D to Q delay.

D. For each of FF 1 and 3, if their hold times are negative (a changing D can still pass through the FF, it does not hold its value after clock rising edge) explain why.
E. For FF 2, find out how much overlap between Phi1 and Ph2 makes it fail.
F. For FF 1, you may find that its performance is worse (larger setup and hold time) for a falling input. Describe how you can skew the 4 inverters along the main path to balance the performance for rising and falling inputs.

5. Pick either FF 1 or FF 3 and lay it out as a standard cell. Explain the reasons for you choice, including, but not limited to, the setup and hold times.