Lab Assignment #2
University of Pittsburgh
Department of Electrical and Computer Engineering

Introduction

This lab follows the pattern of labs we will be using for the rest of the term. In each lab we will ask you to:

1. Learn new information, skills, and tools
2. Use those skills to create, test, and experiment on new designs
3. Analyze and understand the results of the experiments
4. Draw some conclusions from your analysis
5. Write up a report with your results, analysis, and conclusions

Overview

In this lab you will learn about SPICE, develop skills in using schematics entry and simulation in the Cadence environment by working through Tutorials 1 and 2 on our web page, and create three (3) test circuits and perform simulation measurements on them.

Lab Assignment

1. Do Tutorial 1. Note sizes of transistors, size of load, delay and transition times for rising and falling edges.
2. Do tutorial 2. Record currents at four (4) points on the final set of curves.
    a. Use two values for vds: = vdd, vdd/2; and two values for vds = vdd, vdd/2, with vdd = 1.8 Volts.
    b. Compute the slope of the four line segments from 0 to those four points.
    c. Use the slope to compute the effective resistance of the transistor at those four points.
    d. Compare these results with the analytical calculation described in the book example 2.11 note the sizes of the transistors (redo the math).
3. Use the inverter from Tutorial 1 above to build a 7 stage ring oscillator.
    a. Use initial condition control to set one node to 1.8V to force the oscillator to start oscillating.
    b. Measure the frequency and period of the oscillator.
    c. Use this to compute the delay time of the inverter. Note carefully how many transitions in the circuit correspond to one period of the ring oscillator.
4. Analyze and report on:
    a. Ids current computed by equations vs spice traces
    b. Rise, fall and delay times of inverter
5. Write a report <u>(yes a real report, not just some sheets stapled together)</u>
    a. Include printouts of all circuits and printout of waveforms
    b. Include all measurements and calculations
        i. Comparisons of Ids computed vs simulated for selected points
        ii. Comparisons of rise/fall and delay times from different simulations
        iii. Table for Req under different conditions
    c. Conclusions for use in simple linear RC models:
        i. Given Req what value of Cgeq makes sense for the delays observed?

Pay attention to the sizes of the transistors used in these tests and the load that each transistor "sees" in the ring oscillator.

Note: A ring oscillator is a device composed of an odd number of inverters whose output oscillates between two voltage levels, representing true and false. The inverters are attached in a chain and the output of the last inverter is fed back into the first inverter. The schematic for a 7-stage ring oscillator is shown below: